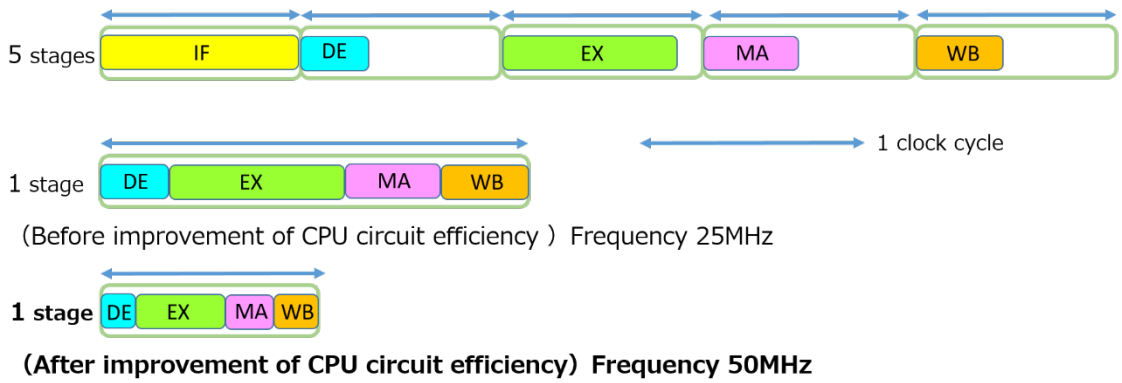
30 April, 2021

Development of highly efficient Single-Stage RISC-V processor to promote the spread of energy harvesting IoT devices

UNO Laboratories, Ltd. is developing a non-pipelined Single-Stage processor with RISC-V (RV 32 IM).
In this study, we have successfully improved the CPU circuit efficiency of the Single-Stage FPGA and achieved twice the operating frequency of the previous verification results (Table 2).
Additionally, by replacing registers which were composed of Flip Flops with BRAM, the logic elements were significantly reduced(*2 ⇒ Table 2).

The advantage of this processor is that the IF stage is eliminated using the patented technology (*1) and the operations are optimized. Please see the below diagram.

【Architecture Comparison Diagram】



【Dhrystone test result on FPGA】

(Table 1) Before CPU circuit efficiency improvement

<Compared on Digilent®Arty A7 : Xilinx®Artix-7 XC7A100T-1CSG324C>

※Operating frequency 100MHz

	1 stage non pipeline PMEM 16KB DMEM 16KB	3stages non pipeline PMEM 16KB DMEM 16KB	3 stages pipeline PMEM 16KB DMEM 16KB
Frequency	25MHz	25MHz	25MHz
DMIPS	33.9	11.9	22.4

（Table 2） **After improvement of CPU circuit efficiency**

＜Compared on Digilent®Arty A7 : Xilinx®Artix-7 XC7A100T-1CSG324C＞

※Operating frequency 100MHz

	1 stage non pipeline PMEM 32KB DMEM 32KB	1 stage non pipeline PMEM 64KB DMEM 32KB	1 stage non pipeline PMEM 128KB DMEM 32KB
Frequency	50MHz	50MHz	40MHz
DMIPS	70.43	70.43	56.34
DMIPS/MHz	1.408	1.408	1.408

※By replacing registers which were composed of Flip Flops with BRAM, the logic elements were significantly reduced.

The Single-Stage architecture returns to the original program in the next clock cycle after the branch or interrupt is completed(*2) so that it does not need to discard the loaded program nor reloaded the program, which prevents operation delay.
This operation improvement realizes low power consumption CPU.
In addition, the Single-Stage architecture is suitable for parallel processing due to its small circuit size and high utility efficiency, and is effective not only for embedding into IoT devices, but also for edge computing in self-driving car and AI that require image processing.

1．Patent Licensing and FPGA IP Core Sales

UNO Laboratories, Ltd. have demonstrated the superiority of the Single-Stage architecture based on its patented technology (*1).
We will license the patented technology and sell IP cores of Single-Stage FPGA to which the patented technology is applied.

2．Implementation in clock synchronous and asynchronous ASIC

The Single-Stage architecture can be universally applied to existing von Neumann computer architectures and can be expected to synergize with other innovative technologies.
To further improve performance, we have a plan to implement the Single-Stage architecture in clock-synchronous and clock-asynchronous ASIC.

One of the most significant advantages of applying a Single-Stage architecture to the development of asynchronous ASIC is eliminating the need for traditional asynchronous circuit design and the availability of synchronous development tools.
The Single-Stage ASIC can be used in sensor nodes with LPWA and other energy-harvesting IoT devices and in a wide range of applications, including automotive devices, aerospace devices, 5G terminals and AI, which require compact, lightweight, low heat generation and stable operation.

Our proposal is low power consumption CPU development. It makes radiation noise reduce, which prevents side-channel attacks. Overall, our product could contribute to realizing a safe and secure IoT society.

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JAPAN	PATENT NUMBER	4862100
USA	PATENT NUMBER	US 8,516,225 B2
TAIWAN	PATENT NUMBER	I -389027
KOREA	PATENT NUMBER	10-1178293

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A Single-Stage RISC-V Processor to Mitigate the Von Neumann Bottleneck

Published in 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS2019)